UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C. 20436

EXHIBIT

Before The Honorable Debra Morriss
Administrative Law Judge

In the Matter of CERTAIN VIDEO GRAPHICS DISPLAY CONTROLLERS AND PRODUCTS CONTAINING SAME	)))))))	Inv. No. 337-TA-412

EXPERT REPORT OF WILLIAM G. MEARS

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EXPERT REPORT OF WILLIAM G. MEARS

I have prepared this expert report at the request of respondent ATI Technologies, Inc. and if called to testify as the contents of the report, could and would testify competently thereto. In this report, I consider issues of validity relating to asserted claims of U.S. Patent No. 5,598,525 ("the '525 patent"). I will describe the 1280 and VIPER series graphics and video controller products that were designed, manufactured, and sold by Parallax Graphics, Inc., a company that I co-founded in 1982. As I detail in my report, the 1280 and VIPER graphics and video controllers contain features and functionality that are described and claimed in the '525 patent. In fact, we at Parallax were implementing the architecture and functionality set forth in the '525 patent many years before the patent. We were years ahead of most others in the industry in our work dealing with the merger of video and graphics.

As fully explained below, I believe that asserted claims of the '525 patent are invalid in view of the 1280/VIPER products. In forming my opinions, I rely on my knowledge and

experience in the field of graphics and video controllers, and on certain documents and information that are specifically referenced in the report. I would like to point out that my work in this case is continuing and that this report represents only a current evaluation of my positions on validity. I may supplement this report as additional information becomes available and my trial testimony may also include additional views developed in connection with my ongoing work in this case. I also may submit a rebuttal expert report regarding any issues raised by Cirrus's experts.

MY GENERAL BACKGROUND

I have over 15 years of experience in video and graphics product development. That experience is summarized in my resume which is attached hereto as Exhibit 1. At the hearing in this case, I may offer testimony relating to my background and experience, some of which is captured in my resume.

Briefly, however, much of my experience derives from my work at Parallax from 1982 through 1991, a company I co-founded. I describe this experience in more detail below. After Parallax, I worked at Force Computers as a manager in the VME Engineering group where I designed and developed VME processor cards that were successfully launched into the market. In early 1994, I started my own contracting business where I worked with a number of companies to develop integrated Computer Graphics/Video products for a variety of applications. In early 1995, I was asked to be Director of R&D at Viewgraphics, Inc. where I developed and brought to market the company's Serial Digital Adapter (SDA) & Digital Data Adaptor (DDA) product families. These products successfully interfaced

broadcast quality real-time video and were successfully introduced to the computer market. I am now Vice-President of Cogent Technology, a company that I have co-founded. At Cogent, I have developed architecture and performed designed work for a MPEG-2 transport stream processing product line. This product line is intended to facilitate the deployment of the digital television broadcast infrastructure. I have a Bachelor of Science in Electrical Engineering from Cornell University.

I am being compensated for my efforts in this case at my standard consulting rate of $250/hr. My compensation in this case is not tied to the result of the litigation.

In the preceding four years, I have not provided any expert testimony at trial or in deposition. In the preceding ten years, to the best of my recollection, I have authored no publications dealing with the subject of graphics and video.

PARALLAX GRAPHICS - THE COMPANY

In 1982, I co-founded Parallax to fill a need in the market for high performance and low cost graphics. We envisioned designing and producing boards that would replace high overhead and high cost "box" like equipment, yet provide at least the same level of functionality and performance of previous generation products. Because of my previous exposure to video, I felt it was critical to integrate video and graphics in the architecture of our products.

In 1982, we designed our first product referred to as the Parallax 600. This product had the ability to capture and display video in real-time and could overlay graphics on a live video background using a simple form of color-keying. This product was successful

predominantly because of its ability to integrate graphics and video. We sold many hundreds of these systems which were used by, for example, Clairol to do visual make-overs of people's images by capturing real-time images and overlaying them with graphical data. The product also captured real-time motion video for overlay. Although the product was successful, it had problems. Specifically, the Parallax 600 processed video in the graphics space. That is, the product used 8 bits per pixel to store both graphics and video data. The color was derived by using RGB format with three bits for red, three for green, and two for blue. This only provided for a total of 256 colors that were used for both video and graphics. This was not enough color subtlety for high quality video.

So we began to explore alternative storage formats for the video data. The human eye sees most detail in terms of black/white images or luminance. Thus, if more bits of storage are allocated to "luma" image and less to the "chroma" image, the resulting data format would be more visually appealing with the same number of bits. This storage data format is well known as YUV in the video industry (and indeed was known in the 1950's during the transition from B/W to color television broadcast). When the data is sampled in the YUV format, only one sample of U & V (or chroma) is needed for each four Y (or luma) samples. For example, across a sample of four pixels there would be four 6 bit luma samples, and one sample of each U & V at a resolution of four bits. The visual perception created a pixel of 16.536 possible different colors, far more than the 256 colors of the previous system. Also, this approach freed the color tables to be available to the user's preference for graphics colors.

We (and. in particular. I) applied these principles to the design and architecture of a next generation product referred to as the 1280. Design for this product began by early 1984. In designing the 1280, we had several design goals in mind: (1) display resolution at 1280 x 1024; (2) ability to capture and display with enhanced resolution as compared to the 600; (3) increased graphics performance with increased off-screen memory; (4) and increased integration to reduce product size and power demands. With these objectives, we designed an architecture for the 1280.

The design of the new video encoding format, as well as the ability to display video on a high resolution display was innovative and deemed patentable at the time. However, Parallax Graphics chose to use protection of trade secrets as our operating paradigm, rather than pursue patents for the purpose of protection. As described below, however, there are contemporaneous documents describing the operation of our products.

During this time frame (early to mid 1984), we also had discussions with Martin Marietta about implementing our design and architecture in conjunction with products produced by them. In this regard, Martin Marietta actually participated in the design specifications for the 1280 in order to ensure that our product would meet their needs. Martin Marietta was developing a portable tactical computer that used video discs to store maps, a product referred to as ASAS. This product was being designed for the military. The 1280 was to be the display for the ASAS work station, and was required to capture live video, and overlay graphics onto the video. Because of their need to display graphics over video, we

enhanced our design to include "graphics-over-video" features. These enhancements included the ability to draw graphics directly over the video. in addition to having video windows.

The result of our efforts were completed sometime in 1985 and in 1986 we were shipping the product to customers, including Martin Marietta. A write up of our product appeared in a March 25, 1986 article entitled "Coprocessors Provide Integrated Video and Graphics," written by Marty Picco, a co-founder of Parallax.

The 1280 series graphics processor was very successful, particularly because of its unique ability to capture and display live video. For example, Boeing used it to dramatically improve its documentation for its 747. Boeing used the 1280 to create laser disc based manuals that replaced the paper manuals previously used at Boeing, which filled a tractor-trailer. The system was implemented by Boeing to display textual description of procedures relating to its many thousands of parts and would display an instructional video along side graphics and text. Our controllers were also used to pilot remote control robots used in the clean-up of the Three Mile Island nuclear accident. To the best of my recollection, other customers include Electronic Data Systems, the Israeli Ministry of Defense, and Texas Instruments. The 1280 was designed for use in Q-Bus and VME workstations from companies like Digital Equipment Corp., and Sun; there was also a version for IBM PCS. Through the introduction of this product, our annual sales volume increased from relatively little to over three million dollars per year. The products, depending on the configuration, sold from $9,000 to $35,000 each.

The 1280 was successful and possessed many product features not otherwise available in the market place during this period of time. In an effort to keep the 1280 product competitive in the market place, we envisioned a next generation product called the VIPER. This product would reduce the size and cost of the 1280 by consolidating discrete circuitry into gate arrays that reduced the power and space requirements in the design. The VIPER was introduced sometime in 1988. The VIPER is described in a version of its users manual dated 1989 (ATI031566-ATI032067). A picture of the VIPER displaying graphics and multiple video windows is depicted in a 1989 publication entitled The NEWS Book. We were selling an average of 50 VIPER controllers per month during this time period and our annual revenues increased to 9 to 10 million dollars per year. I note that at this period of time, the market began to see the emergence of windowing systems such as NEWS for Sun workstations and "X" for DEC workstations. Our product was used with both which further enhanced our sales.

The success of the Parallax 1280 and VIPER products did not go unnoticed in the industry. In 1989, we were acquired by a company called Dynatech Corporation, a 400 million dollar publicly traded company, which continued to sell the product. I left the company in 1991.

PARALLAX - THE PRODUCTS

The Parallax 1280/VIPER series graphics and video processors can be understood with reference to a Parallax 1280 technical manual (ATI032068-ATI032775); a Parallax VIPER technical manual (ATI031566-ATI032067); an excerpt from The News Book at pp. 178-221

(ATI0___-ATI0___); and a March 25,1986 Digital Design article entitled "Coprocessors Provide Integrated Video and Graphics." by Marty Picco (a co-founder of Parallax). I also have in my possession sample 1280 and VIPER boards.

A. THE 1280 SERIES

The architecture and functionality of the 1280 series controller is now described. The architecture can best be understood by considering its different functional blocks. In the Parallax 1280 technical manual (ATI032068-ATI032775), there is a high level functional block diagram that generally depicts the functionality of the 1280 product. <u>See</u> Figure H-5 on page H-27 (ATI032738). For purposes of this discussion, I will consider the following functional blocks: (1) control/processor section (2) display memory section; (3) video input section; and (4) display generation section.

The control processor section consisted of a core processor that was responsible for choreographing all operations of the controller. The core processor accepted high level instructions from the host and translated them into multiple low-level read and write instructions that were issued to the display memory circuitry. The host sent both graphics and video data to the core processor over the system bus. More specifically, the graphics or video data from the host was received by the Bus Interface Unit (BIU), which is a multi-aperture port. As well as converting host commands, the core processor was also responsible for controlling the display generation circuitry. Additionally, the core processor also directed the read out of data from memory.

The core processor performed various manipulations on display memory which included (1) writing a single pixel; (2) writing a horizontal run of solid color pixels of programmable length and position; (3) writing a repeating pattern of pixels (STIPPLE); (4) copying a horizontal run of pixels from one area in memory (such as off-screen) to another; (5) and importing horizontal run from the real-time video interface. As well as controlling what pixels were written, the core processor also had control over the Access Attribute Control, which had the role of modifying and enabling the writing of each pixel on an individual basis according to the mapping specified by the Access Attribute Control.

In the 1280, display memory was interleaved by a factor of eight. This means that eight locations are read or written simultaneously. The interleave was organized horizontally such that a single access to memory would read eight horizontally consecutive pixels. This interleaving was important to achieve the necessary data rates demanded by the display while still retaining sufficient bandwidth for drawing into and modifying display memory. Access to display memory was timed-division-multiplexed, meaning that either the display circuitry or the access circuitry would have sole access that was traded off as necessary. The display circuitry, however, always had priority.

The display memory (or frame buffer) of the 1280 had a dimension of 2048 x 2048, or 320 percent of the memory necessary for a 1280 x 1024 display. The frame buffer had on-screen and off-screen memory that each stored any kind of data including video and graphics data. The frame buffer also stored the graphics and video data in their respective graphics and video formats (i.e. RGB for graphics and YUV for video). The frame buffer had no

restriction on the size or position of the video or graphics areas (other than video areas needed to start and end on multiples of 4 pixels horizontally). While the standard configuration of the product employed an 8 bit depth of the display memory, we also offered 16 and 24 bit versions of the product to certain customers who demanded it. With this extended memory option, certain additional display features were made available.

The 1280 also had a real-time video port as shown in the Figure. The function of this port was to decode an analog RS170 color video signal and convert it to a digital bit stream. Synchronization information from the analog signal was separated from image data and sent to the control processor that managed the frame grabbing process. The control processor also included circuitry that generated a memory address for the video data. The image data was formatted into video mode byte stream that was written directly into the display memory during the frame grabbing process.

Finally, the display generation circuitry of the 1280 is described. This circuitry performed two basic functions: (1) control the timing and synchronization of memory retrieval from the frame buffer to the raster scan of the display monitor and (2) process the stream of pixels as either video format pixels or graphics, and deliver them to the monitor at the appropriate time.

The timing and synchronization circuitry used an origin register that was written by the core processor. The origin register included the number of lines of data to be displayed from that origin. When the display of those lines were completed, the display generator would interrupt the core processor for the next display segment. This technique permitted the

screen to be split into multiple independent display regions. As well as controlling split screen operations, the control processor programmed a SYNC generator with appropriate monitor parameters.

While only 1280 x 1024 pixels were displayable in any given frame, ALL of the display memory was viewable by simply changing the values loaded into the display origin register. This means that graphics and video format data stored in off-screen memory could be easily displayed without copying it to the on-screen area of memory.

The second part of the display circuitry processed the stream of pixels. Pixels were processed as either video or graphics depending on the value of the display attribute map (DAM). This extra bit plane in the frame buffer was used to distinguish areas of video format data from areas of graphics format data. The display stream hardware was comprised of two pipelines: one pipeline for video and one pipeline for graphics. The graphics pipeline passed each pixel through an 8 x 24 color look up table yielding a 24 bit RGB pixel. The video pipeline processed the video format data, which included decoding YUV into RGB.

A multiplexer served as data selector, or overlay generator, that would selectively pass data from either the video display pipeline or the graphics display pipeline through to the monitor in a manner that was mode dependent, i.e. graphics mode, video mode, and graphics over video mode. All display memory data was passed to both pipelines; based on the DAM bit, contents from the display memory would be output as either video format data, or as graphics format data. Data output from the other pipeline for that pixel location was simply discarded. In an optional display mode known as graphics over video, bit zero of each

luma sample in the video pipeline acted like a color key. In the case where bit zero was off (i.e. 0), video samples passed through the video pipeline as described above. In the case where bit zero was on (i.e. 1), bits 1-5 were treated as a pseudo color graphics pixel and displayed from the graphics pipeline. Thus, 32 colors were made available to display graphics pixels within a video region on a pixel by pixel basis.

In the case of 16 and 24 bit memory options, the display circuitry could treat graphics areas as true color pixels. This means that if the DAM bit was a 0, that the graphics pixel would be generated in true color mode from a full 16 or 24 bits of display memory. If the DAM bit was a 1, then the video format pixel would be generated exactly as described above.

B. THE VIPER SERIES

As I noted above, we at Parallax created the next generation product called the VIPER in order to reduce power consumption, space requirements, and the cost of the processors to our customers. This was intended to ensure that the 1280 had continued viability into the future. With these design objectives in mind, we modified the 1280 by consolidating discrete circuitry into gate arrays that reduced the power and space requirements in the design. The functionality and architecture of the VIPER is otherwise the same as the 1280. As such, everything I said above with respect to the 1280 equally applies to the VIPER.

C. SUMMARY OF FUNCTIONALITY FOR THE PARALLAX 1280/VIPER PRODUCTS

To summarize the architectural and functional features of the 1280/VIPER, I identify the attributes of the 1280/VIPER products:

(1) The 1280/VIPER merged video and graphics data from a single multi-format

frame-buffer for simultaneous display on a computer monitor. Multiple video windows could appear anywhere on the display monitor. There was no specific correspondence between the location of the video data stored in the frame buffer and the location of the video window on the monitor.

(2) The 1280/VIPER had a multi-aperture port for receiving both video and graphics data from the system bus. The arriving data had a host assigned address that was temporarily stored in an address buffer.

(3) The 1280/VIPER used a single frame buffer to store both video and graphics data in their native formats (i.e. RGB and pseudo-color for graphics and YUV for video). The frame buffer had on-screen and off-screen areas. Also, YUV video data could be stored in either off-screen or on-screen memory and RGB graphics data could be stored in either on-screen and off-screen memory.

(4) The 1280/VIPER contained circuitry for writing into on-screen and off-screen areas of the frame buffer. The 1280/VIPER also contained circuitry for selectively retrieving data from on-screen and off-screen portions of the memory and directing the data to the back-end graphics and video pipelines.

(5) The 1280/VIPER had a graphics over video mode that utilized a version of color keying to overlay video with graphics. In other modes, the control overlay circuitry switched data streams at the output with the presence of the DAM bit.

(6) The 1280/VIPER has a real-time video port that decoded analog RS170 color video signal and converted it to a digital bit stream in a YUV format. The control processor

also included circuitry that generated a memory address for the video data. The image data was formatted into a video format byte stream which was written directly into the display memory during the frame grabbing process.

THE '525 PATENT

The '525 patent is entitled "Apparatus, System and Method For Controlling Graphics And Video Data in Multimedia Data Processing And Display Systems," and issued on January 28, 1997. The '525 patent contains a total of 47 claims with claims 1, 13, 25, 34, 37, and 43 being independent claims. In the hearing in this case, I may offer testimony generally describing the '525 patent from the perspective of one skilled in the art.

I understand that a patent claim is invalid based on anticipation if one prior art reference or product includes all the limitations of that claim. I also understand that a patent claim is invalid based on obviousness in view of one or more prior art references. I am told that when examining the question of obviousness, one must consider the following factors: scope and content of the prior art; level of skill in the art; differences, if any, between the invention claimed and the prior art; secondary considerations including commercial success, copying, long-felt need, and other independent development of the claimed invention. I am also told that obviousness must be tested as of the time the invention was made. One must ask the questions, "Would this have been obvious to a person having ordinary skill in the art at the time the invention was made?" I am also told that the test for obviousness is what the combined teachings of the references would have suggested, disclosed, or taught to one of ordinary skill in the art.

I also understand that the plaintiff in this case claims to have made the invention of the '525 patent in September 1993. At that time, the level of skill in the art of graphics controller development and also the art of video product development was quite high. At the same time, the multimedia market was expanding quite quickly, creating an incentive to provide products which combined video with graphics. There was a large demand for designers with overlapping skills. A person of ordinary skill in this combined area would have experience designing graphics controllers as well as video processing circuits and would have been familiar with many different design choices. I was such a designer, and at the time, knew other designer with similar skills in the art of video/graphics controllers. In the following chart, I compare the elements of the claims of the '525 patent with the Parallax 1280/VIPER products and with my knowledge of ordinary skill in the graphics/video art. In doing so, I interpret the words of the claims according to their ordinary meanings to me as an engineer. I am not a lawyer and am not attempting to give legal meaning to the claims. I understand that doing so requires consideration of the patent specification, the patent prosecution history, and numerous legal principles. I have read the patent specification but not the prosecution history. Once the claims have been legally construed in this case, I reserve the right to modify the chart below. I also must again stress that my investigation is continuing, and that additions and/or deletions may be made in the future and reflected in my trial testimony. For trial, I may also prepare diagrams, other charts, and possibly a demonstration that illustrates the architecture and operation of the Parallax products.

APPLICATION OF THE PARALLAX 1280/VIPER TO THE ASSERTED CLAIMS

CLAIM 37 IS INVALID OVER PARALLAX

CLAIM 37	PRIOR ART
37. A display controller comprising:	Parallax 1280/VIPER
circuitry for selectively retrieving data from an associated multi-format frame buffer for simultaneously storing graphics and video data;	circuitry in Parallax 1280/VIPER for selectively retrieving graphics (RGB) and video (YUV) data from display memory.
a first pipeline for processing words of graphics data selectively retrieved from said frame buffer; and	circuitry in Parallax 1280/VIPER for processing graphics (RBG) data
a second pipeline for processing words of video data selectively retrieved from said frame buffer.	circuitry in Parallax 1280/VIPER for processing video (YUV) data

CLAIM 43 IS INVALID OVER PARALLAX

CLAIM 43	PRIOR ART
43. A display controller for interfacing a multi-format frame buffer and a display device. the multi-format frame buffer having on-screen and off-screen areas each for simultaneously storing both graphics and video pixel data, said display controller comprising:	Parallax 1280/VIPER, with frame buffer for simultaneously storing graphics (RGB) and video (YUV), each in on-screen or off-screen areas
circuitry for selectively retrieving pixel data from a selected one of said on-screen and off-screen areas of said frame buffer;	circuitry in Parallax 1280/VIPER for selectively retrieving graphics (RGB) and video (YUV) data, from either on-screen or off-screen regions of the frame buffer
a graphics backend pipeline for processing graphics data retrieved from said selected one of said areas of said frame buffer;	circuitry in Parallax 1280/VIPER for processing graphics (RBG) data

a video backend pipeline for processing video data retrieved from said selected one of said areas of said frame buffer; and	circuitry in Parallax 1280/VIPER for processing video (YUV) data
an output selector for selectively passing to said display device data received from said graphics or video backend pipelines.	circuitry in Parallax 1280/VIPER for selecting between graphics/video pipelines (overlay generator, or multiplexer)

CLAIM 1 IS INVALID OVER PARALLAX

CLAIM 1	PRIOR ART
1. A graphics and video controller comprising:	Parallax 1280/VIPER
an interface for receiving words of pixel data, each said word associated with an address buffer;	circuitry in Parallax 1280/VIPER for receiving pixel data
circuitry for writing each said word of said pixel data received by said interface to a one of on-screen and off-screen memory areas of a frame buffer;	circuitry in Parallax 1280/VIPER for writing pixel data into on-screen and off-screen regions of the frame buffer
circuitry for selectively retrieving said words from said on-screen and off-screen area;	circuitry in Parallax 1280/VIPER for selectively retrieving pixel data from on-screen and off-screen regions of the frame buffer
a first pipeline for processing words of graphics data retrieved from said frame buffer;	circuitry in Parallax 1280/VIPER for processing graphics (RBG) data
a second pipeline for processing words of video data retrieved from said frame buffer.	circuitry in Parallax 1280/VIPER for processing video (YUV) data

CLAIM 2 IS INVALID OVER PARALLAX

CLAIM 2	PRIOR ART
2. The controller of claim 1 and further comprising output selection circuitry for selecting for output between graphics data received from said first pipeline and data received from said second pipeline, said selection circuitry operable to:	circuitry in Parallax 1280/VIPER for selecting between graphics and video pipelines
in a first mode, pass data from said first pipeline; and	circuitry in Parallax 1280/VIPER for passing data from graphics pipeline
in a second mode, pass data from said second pipeline when said data corresponds to a selected display position of a display window.	circuitry in Parallax 1280/VIPER for passing data from video pipeline when in a video region

CLAIM 3 IS INVALID OVER PARALLAX

CLAIM 3	PRIOR ART
3. The controller of claim 2 wherein said selection circuitry is further operable to:	

in a third mode, pass data from said second pipeline when said data corresponds to said selected display position of said display window and data from said first pipeline match a color key.	circuitry in Parallax 1280/VIPER for passing data from video pipeline when in a video region and based on graphics over video keying control In Parallax 1280/VIPER, overlay of video onto graphics with video-based keying was accomplished with Access Attribute control during a copy or frame grabbing operation. This technique differed from the popular "color-key blue" which was well known in the art, while still solving customer needs for keying of video over graphics. Parallax's choice to key graphics OVER video was a design decision based on customer needs. Nothing unique about this choice over decision to overlay video onto graphics.

CLAIM 4 IS INVALID OVER PARALLAX

CLAIM 4	PRIOR ART
4. The controller of claim 3 wherein said selection circuitry is further operable in a fourth mode to pass data from said second pipeline when data from said first pipeline match a color key.	circuitry in Parallax 1280/VIPER for passing data from video pipeline based on graphics over video keying control In Parallax 1280/VIPER, overlay of video onto graphics with video-based keying was accomplished with Access Attribute control during a copy or frame grabbing operation. This technique differed from the popular "color-key blue" which was well known in the art, while still solving customer needs for keying of video over graphics. Choice to key graphics OVER video was a design decision based on customer needs. Nothing unique about this choice over decision to overlay video onto graphics.

CLAIM 5 IS INVALID OVER PARALLAX

CLAIM 5	PRIOR ART
5. The controller of claim 1 wherein said circuitry for retrieving maintains a stream of graphics data to said first pipeline and provides video data to said second pipeline when a display raster scan reaches said display position of said window.	circuitry in Parallax 1280/VIPER for passing graphics data to graphics pipeline and for passing video data to video pipeline when in a video region Position of video region was indicated by DAM bit in addition to position on raster display scan.

CLAIM 6 IS INVALID OVER PARALLAX

CLAIM 6	PRIOR ART
6. The controller of claim 1 and further comprising:	
a video port for receiving real-time video data; and	circuitry in Parallax 1280/VIPER for receiving real-time video
circuitry for generating an address to said memory at which said real-time video data is to be stored.	circuitry in Parallax 1280/VIPER for generating addresses for received real-time video data

CLAIM 7 IS INVALID OVER PARALLAX

CLAIM 7	PRIOR ART
7. The controller of claim 1 wherein said second pipeline includes a first first-in-first-out memory for receiving data for a first display line of pixels in memory and a second display line of pixels memory.	Parallax hardware employed first-in-first-out buffering between the display memory and the display monitor for the graphics format data and the video format data. Parallax's implementation required only one line of buffering outside the display memory. The addition of a second FIFO buffer would be a requirement of the design implementation, NOT a unique invention.

CLAIM 8 IS INVALID OVER PARALLAX

CLAIM 8	PRIOR ART
8. The controller of claim 7 wherein said first display line adjacent in memory to said second display line.	Parallax hardware employed first-in-first-out buffering between the display memory and the display monitor for the graphics format data and the video format data. In the event that a given design would need more than a single line of buffering, it would be obvious that the second line of buffering be adjacent to the first (and below the first).

CLAIM 9 IS INVALID OVER PARALLAX

CLAIM 9	PRIOR ART
9. The controller of claim 7 wherein said output selection circuitry comprises:	

an output selector for selecting between data from said second pipeline and data from said first pipeline in response to a selection control signal:	circuitry in Parallax 1280/VIPER for selecting between graphics/video pipelines (overlay generator, or multiplexer)
a register for maintaining a plurality of overlay control bits;	register of plural control bits in Parallax 1280/VIPER There is nothing inventive about the use of a register to hold control bits. Parallax implemented a register specific to the control of the video/graphics MUX.
window position control circuitry for selectively generating a position control signal when a word of said data stream from said second pipeline falls within a display window;	circuitry in Parallax 1280/VIPER for passing data from video pipeline when in a video region Position of video region was indicated by DAM bit in addition to position on raster display scan.
color comparison circuitry for comparing words of said data stream from said first pipeline with a color key and for providing in response a color comparison control signal; and	circuitry in Parallax 1280/VIPER for passing data from video pipeline based on graphics over video keying control In Parallax 1280/VIPER, overlay of video onto graphics with video-based keying was accomplished with Access Attribute control during a copy or frame grabbing operation. This technique differed from the popular "color-key blue" which was well known in the art, while still solving customer needs for keying of video over graphics. Choice to key graphics OVER video was a design decision based on customer needs. Nothing unique about this choice over decision to overlay video onto graphics.

a control selector for selectively providing a said selection control signal in response to said overlay control bits in said register and at least one of said position control and color comparison control signals.	circuitry in Parallax 1280/VIPER for passing data from video pipeline when in a video region and based on graphics-over-video keying control bit. This functionality was selectively provided in response to overlay control bits from the overlay control register. In addition, overlay controls were well known in art, and it was well known in art to store control bits in a register.

CLAIM 10 IS INVALID OVER PARALLAX

CLAIM 10	PRIOR ART
10. The controller of claim 9 wherein said window position control circuitry comprises:	
window position counters operable to increment from initial count values corresponding to a starting pixel of a display window as data representing each pixel in a display screen is pipelined through said overlay control circuitry;	window position counters in the Parallax 1280/VIPER for the generation of coherent pixel display streams (which is well known art in graphics controllers). Parallax 1280/VIPER hardware was able to maintain a plurality of video display start coordinates within a single display, each with arbitrary X and Y origins.
screen position counters operable to count as data representing each pixel in said display screen is pipelined through said overlay control circuitry; and	window position counters in the Parallax 1280/VIPER for the generation of coherent pixel display streams (which is well known art in graphics controllers). Parallax 1280/VIPER hardware was able to maintain a plurality of video display start coordinates within a single display, each with arbitrary X and Y origins

comparison circuitry operable to compare a current count in said window position counters and a current count in said screen position counters and selectively generate said position control signal in response.	circuitry in Parallax 1280/VIPER for loading counters with difference. and comparing result to zero This form of compare circuit is well known in the art.

CLAIM 12 IS INVALID OVER PARALLAX

CLAIM 12	PRIOR ART
12. The controller of claim 1 wherein said interface includes a dual-aperture port.	circuitry in Parallax 1280/VIPER for receiving graphics and video data through multi-aperture port

CLAIM 13 IS INVALID OVER PARALLAX

13. A controller comprising:	
circuitry for writing selectively each word of received data into [a] selected one of on-screen and off-screen memory spaces of a frame buffer:	circuitry in Parallax 1280/VIPER qualifying each write to on-screen and off-screen areas of display memory through the Access Attribute Control
a first port for receiving video and graphics data. a word of said data received with an address of said memory spaces directing said word to be processed as a word of video data or a word of graphics data;	circuitry in Parallax 1280/VIPER for receiving graphics and video data and directing that it be stored and displayed as video or graphics
a second port for receiving real-time video data:	circuitry in Parallax 1280/VIPER for receiving real-time video data
circuitry for generating an address associated with a selected one of said memory spaces for a work of said real-time video data;	circuitry in Parallax 1280/VIPER for generating addresses for received real-time video data

circuitry for selectively retrieving said words of data from said on-screen and off-screen memory spaces as data is rastered for driving a display;	circuitry in Parallax 1280/VIPER for selectively retrieving graphics (RGB) and video (YUV) data. from either on-screen or off-screen regions of the frame buffer
a graphics backend pipeline for processing ones of said words of data representing graphics data retrieved from said frame buffer;	circuitry in Parallax 1280/VIPER for processing graphics (RBG) data
a video backend pipeline for processing other ones of said words of data representing video data retrieved from said frame buffer. said circuitry for retrieving always rastering a stream of data from said frame buffer to said graphics backend pipeline and rastering video data to said video backend pipeline when a display raster scan reaches a display position of a window; and	circuitry in Parallax 1280/VIPER for processing video (YUV) data, for passing graphics data to graphics pipeline, and for passing data to video pipeline when in a video region. Position of video region was indicated by DAM bit in addition to position on raster display scan.
output selector circuitry for selecting for output between works of data output form said graphics backend pipeline and words of data output from said video backend pipelıne.	circuitry in Parallax 1280/VIPER for selecting between graphics/video pipelines (overlay generator, or multiplexer)

CLAIM 14 IS INVALID OVER PARALLAX

CLAIM 14	PRIOR ART
14. The controller of claim 13 wherein said output selector is further operable to select between graphics data output from a color look-up table and true color data output from said graphics pipeline.	circuitry in Parallax 1280/VIPER for processing graphics data as either 24-bit true color or 8-bit color look-up table data

CLAIM 15 IS INVALID OVER PARALLAX

CLAIM 15	PRIOR ART
15. The controller of claim 13 wherein said output selector is operable to:	
in a first mode pass only a word of data output from said graphics pipeline;	circuitry in Parallax 1280/VIPER for passing data from graphics pipeline
in a second mode pass a word of data output from said video pipeline when said display raster scan has reached a display position corresponding to a window and a word of data from said graphics pipeline when said display raster scan is in any other display position;	circuitry in Parallax 1280/VIPER for passing data from video pipeline when in a video region and from graphics pipeline elsewhere
in a third mode pass a word of data output from said video pipeline when said display raster scan has reached a display position corresponding to a window and a corresponding word of data from said graphics pipeline matches a color key and a word of data from said graphics pipeline when said display raster scan is in any other display position; and	circuitry in Parallax 1280/VIPER for passing data from video pipeline when in a video region and based on graphics over video keying control and from graphics pipeline elsewhere In Parallax 1280/VIPER, overlay of video onto graphics with video-based keying was accomplished with Access Attribute control during a copy or frame grabbing operation. This technique differed from the popular "color-key blue" which was well known in the art, while still solving customer needs for keying of video over graphics. Choice to key graphics OVER video was a design decision based on customer needs. Nothing unique about this choice over decision to overlay video onto graphics.

in a fourth mode pass a word of data from said video pipeline when said corresponding word of data from said graphics pipeline matches a color key and a word of data from said graphics pipeline when said display raster scan is in any other display position.	circuitry in Parallax 1280/VIPER for passing data from video based on graphics over video keying control and from graphics pipeline elsewhere In Parallax 1280/VIPER, overlay of video onto graphics with video-based keying was accomplished with Access Attribute control during a copy or frame grabbing operation. This technique differed from the popular "color-key blue" which was well known in the art, while still solving customer needs for keying of video over graphics. Choice to key graphics OVER video was a design decision based on customer needs. Nothing unique about this choice over decision to overlay video onto graphics.

CLAIM 16 IS INVALID OVER PARALLAX

CLAIM 16	PRIOR ART
16. The controller of claim 13 wherein said video pipeline includes a first first-in-first-out memory for receiving a plurality of words of data for a first display line of pixels in memory and a second first-in-first-out memory or receiving a plurality of words of data from a second display line of pixels in memory.	Parallax 1280/VIPER hardware employed first-in-first-out buffering between the display memory and the display monitor for the graphics format data and the video format data. Parallax's implementation required only one line of buffering outside the display memory. The addition of a second FIFO buffer would be a requirement of the design implementation, NOT a unique invention.

CLAIM 17 IS INVALID OVER PARALLAX

CLAIM 17	PRIOR ART
17. The controller of claim 16 wherein said first display line is stored adjacent in memory to said second display line.	Parallax 1280/VIPER hardware employed first-in-first-out buffering between the display memory and the display monitor for the graphics format data and the video format data. In the event that a given design would need more than a single line of buffering, it would be obvious that the second line of buffering be adjacent to the first (and below the first).

CLAIM 18 IS INVALID OVER PARALLAX

CLAIM 18	PRIOR ART
18. The controller of claim 13 wherein said output selector circuitry comprises:	
a control selector having a plurality of control inputs coupled to a register said register storing a plurality of overlay control bits:	circuitry in Parallax 1280/VIPER for passing data from video pipeline when in a video region and based on graphics-over-video keying control bit. This functionality was selectively provided in response to overlay control bits from the overlay control register. In addition, overlay controls were well known in art, and it was well known in art to store control bits in a register.

window position control circuitry coupled to a first control input of said control selector, said window position control circuitry operable to selectively provide a first control signal to said first control input when a word of data being pipelined through said video pipeline falls within a display window;	circuitry in Parallax 1280/VIPER for passing data from video pipeline when in a video region Position of video region was indicated by DAM bit in addition to position on raster display scan.
color comparison circuitry operable to compare a word of data being pipelined through said graphics pipeline with a color key and provide in response a second control signal to a second control input of said control selector; and	circuitry in Parallax 1280/VIPER for passing data from video pipeline based on graphics over video keying control In Parallax 1280/VIPER, overlay of video onto graphics with video-based keying was accomplished with Access Attribute control during a copy or frame grabbing operation. This technique differed from the popular "color-key blue" which was well known in the art, while still solving customer needs for keying of video over graphics. Choice to key graphics OVER video was a design decision based on customer needs. Nothing unique about this choice over decision to overlay video onto graphics.
wherein said control selector is operable to provide an output selection control signal in response to at least one of said first and second control signals and said overlay control bits being stored in said register.	circuitry in Parallax 1280/VIPER for selecting between graphics/video pipelines (overlay generator, or multiplexer) This functionality was selectively provided in response to overlay control bits from the overlay control register. In addition, overlay controls were well known in art, and it was well known in art to store control bits in a register.

CLAIM 19 IS INVALID OVER PARALLAX

CLAIM 19	PRIOR ART
19. The circuitry of claim 18 wherein said output selector circuitry further includes at third control input coupled to certain bits of said graphics pipeline, said output selector further operable to select between data on said respective video and graphics pipelines in response to said certain bits presented to said selector circuitry.	circuitry in Parallax 1280/VIPER for selecting between graphics/video pipelines (overlay generator, or multiplexer) In the event that a given design would need more than two control variables, it would be obvious to use a third control signal.

CLAIM 20 IS INVALID OVER PARALLAX

CLAIM 20	PRIOR ART
20. The circuitry of claim 18 wherein said window position control circuitry comprises:	
a window x-position counter operable to count from a loaded x-position value in response to a video clock, said x-position counter reloading in response to display horizontal synchronization signal;	window position counters in the Parallax 1280/VIPER for the generation of coherent pixel display streams (which is well known art in graphics controllers). Parallax 1280/VIPER hardware was able to maintain a plurality of video display start coordinates within a single display, each with arbitrary X and Y origins.
a window y-position counter operable to count from a loaded y-position value in response to said horizontal synchronization signal. said y-position counter reloading in response to a display vertical synchronization signal;	window position counters in the Parallax 1280/VIPER for the generation of coherent pixel display streams (which is well known art in graphics controllers). Parallax 1280/VIPER hardware was able to maintain a plurality of video display start coordinates within a single display, each with arbitrary X and Y origins.

CRT position circuitry operable maintain counts corresponding to a current display pixel; and	window position counters in the Parallax 1280/VIPER for the generation of coherent pixel display streams (which is well known art in graphics controllers). Parallax 1280/VIPER hardware was able to maintain a plurality of video display start coordinates within a single display, each with arbitrary X and Y origins.
comparison circuitry operable to compare current counts in said window counters with said current counts held in said CRT position circuitry and generate in response said first control signal.	circuitry in Parallax 1280/VIPER for loading counters with difference, and comparing result to zero This form of compare circuit is well known in the art.

CLAIM 21 IS INVALID OVER PARALLAX

CLAIM 21	PRIOR ART
21. The circuitry of claim 20 wherein said window position control circuitry further comprises an x-position register for holding said x-position value for loading into said x-position counter and a y-position register for holding said y-position value for loading into said y-position counter.	window position counters in the Parallax 1280/VIPER for the generation of coherent pixel display streams (which is well known art in graphics controllers). Placing registers to store load values for counters is not inventive, and had been implemented many times by Parallax's hardware design engineers. Parallax 1280/VIPER hardware was able to maintain a plurality of video display start coordinates within a single display, each with arbitrary X and Y origins.

CLAIM 23 IS INVALID OVER PARALLAX

CLAIM 23	PRIOR ART
23. The circuitry of claim 13 wherein said video pipeline comprises:	
a first-in/first-out memory for receiving a first stream of words of data from said frame buffer;	Parallax 1280/VIPER hardware employed first-in-first-out buffering between the display memory and the display monitor for the graphics format data and the video format data.
a second first-in/first-out memory disposed in parallel with said first first-in/first-out memory for receiving a second stream of words of data from said frame buffer; and	Parallax 1280/VIPER hardware employed first-in-first-out buffering between the display memory and the display monitor for the graphics format data and the video format data. Parallax's implementation required only one line of buffering outside the display memory. The addition of a second FIFO buffer would be a requirement of the design implementation, NOT a unique invention.
interpolation circuitry for selectively generating an additional word of data by interpolating a word of said first stream and a word of second stream data output from said first and second first-in/first-out memories.	Parallax's implementation did not interpolate display lines between sampled lines. Parallax's implementation used direct samples from the line above or the line below. However, use of interpolation filters for spatially expanding a display area was well known art as of September 1993, and can be found in numerous video special effect generators (for example Abekas 8150).

CLAIM 24 IS INVALID OVER PARALLAX

CLAIM 24	PRIOR ART
24. The controller of claim 13 wherein said first port comprises a dual-aperture port.	circuitry in Parallax 1280/VIPER for receiving graphics and video data through multi-aperture port

I understand that I may be asked to prepare a rebuttal report and/or give rebuttal testimony at a hearing on matters not covered in this expert report. Additionally, I understand that discovery has not been completed and that I will consider additional evidence in connection with the issues discussed above. After considering any such additional evidence, I may supplement this report as necessary.

Respectfully submitted,

Date: November 17, 1998

William G. Mears

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